SEMESTER -3

ECT201	SOLID STATE DEVICES	CATEGORY	L	T	P	CREDIT
		PCC	3	1	0	4

Preamble: This course aims to understand the physics and working of solid state devices.

Prerequisite: EST130 Basics of Electrical and Electronics Engineering

Course Outcomes: After the completion of the course the student will be able to

CO 1	Apply Fermi-Dirac Distribution function and Compute carrier concentration at equilibrium and the parameters associated with generation, recombination and transport mechanism
CO 2	Explain drift and diffusion currents in extrinsic semiconductors and Compute current density due to these effects.
CO 3	Define the current components and derive the current equation in a pn junction diode and bipolar junction transistor.
CO 4	Explain the basic MOS physics and derive the expressions for drain current in linear and saturation regions.
CO 5	Discuss scaling of MOSFETs and short channel effects.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	3										
CO 2	3	3										
CO 3	3	3										
CO 4	3	3										
CO 5	3											

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember	10	10	20
Understand	25	25	50
Apply	15	15	30
Analyse			
Evaluate			
Create			

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1): Compute carrier concentration at equilibrium and the parameters associated with generation, recombination and transport mechanism

1. Derive the expression for equilibrium electron and hole concentration.

2. Explain the different recombination mechanisms

3. Solve numerical problems related to carrier concentrations at equilibrium, energy band diagrams and excess carrier concentrations in semiconductors.

Course Outcome 2 (CO2) : Compute current density in extrinsic semiconductors in specified electric field and due to concentration gradient.

1. Derive the expression for the current density in a semiconductor in response to the applied electric field.

2. Derive the expression for diffusion current in semiconductors.

3. Show that diffusion length is the average distance a carrier can diffuse before recombining.

Course Outcome 3 (CO3): Define the current components and derive the current equation in a pn junction diode and bipolar junction transistor.

1. Derive ideal diode equation.

2. Derive the expression for minority carrier distribution and terminal currents in a BJT.

3. Solve numerical problems related to PN junction diode and BJT.

Course Outcome 4 (CO4): Explain the basic MOS physics with specific reference on MOSFET characteristics and current derivation.

1. Illustrate the working of a MOS capacitor in the three different regions of operation.

2. Explain the working of MOSFET and derive the expression for drain current.

3. Solve numerical problems related to currents and parameters associated with MOSFETs.

Course Outcome 5 (CO5): Discuss the concepts of scaling and short channel effects of MOSFET.

1. Explain the different MOSFET scaling techniques.

2. Explain the short channel effects associated with reduction in size of MOSFET.

SYLLABUS

MODULE I

Elemental and compound semiconductors, Intrinsic and Extrinsic semiconductors, concept of effective mass, Fermions-Fermi Dirac distribution, Fermi level, Doping & Energy band diagram, Equilibrium and steady state conditions, Density of states & Effective density of states, Equilibrium concentration of electrons and holes.

Excess carriers in semiconductors: Generation and recombination mechanisms of excess carriers, quasi Fermi levels.

MODULE II

Carrier transport in semiconductors, drift, conductivity and mobility, variation of mobility with temperature and doping, Hall Effect.
Diffusion, Einstein relations, Poisson equations, Continuity equations, Current flow equations, Diffusion length, Gradient of quasi Fermi level

MODULE III

PN junctions : Contact potential, Electrical Field, Potential and Charge distribution at the junction, Biasing and Energy band diagrams, Ideal diode equation.
Metal Semiconductor contacts, Electron affinity and work function, Ohmic and Rectifying Contacts, current voltage characteristics.
Bipolar junction transistor, current components, Transistor action, Base width modulation.

MODULE IV

Ideal MOS capacitor, band diagrams at equilibrium, accumulation, depletion and inversion, threshold voltage, body effect, MOSFET-structure, types, Drain current equation (derive)-linear and saturation region, Drain characteristics, transfer characteristics.

MODULE V

MOSFET scaling – need for scaling, constant voltage scaling and constant field scaling.

Sub threshold conduction in MOS.
Short channel effects- Channel length modulation, Drain Induced Barrier Lowering, Velocity Saturation, Threshold Voltage Variations and Hot Carrier Effects.
Non-Planar MOSFETs: Fin FET –Structure, operation and advantages

Text Books

1. Ben G. Streetman and Sanjay Kumar Banerjee, Solid State Electronic Devices, Pearson 6/e, 2010 (Modules I, II and III)

2. Sung Mo Kang, CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill, Third Ed., 2002 (Modules IV and V)

Reference Books

1. Neamen, Semiconductor Physics and Devices, McGraw Hill, 4/e, 2012
2. Sze S.M., Semiconductor Devices: Physics and Technology, John Wiley, 3/e, 2005
3. Pierret, Semiconductor Devices Fundamentals, Pearson, 2006
4. Sze S.M., Physics of Semiconductor Devices, John Wiley, 3/e, 2005
5. Achuthan, K N Bhat, Fundamentals of Semiconductor Devices, 1e, McGraw Hill,2015
6. Yannis Tsividis, Operation and Modelling of the MOS Transistor, Oxford University Press.
7. Jan M.Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Digital Integrated Circuits - A Design Perspective, PHI.

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**MODULE 1**	
1.1	Elemental and compound semiconductors, Intrinsic and Extrinsic semiconductors, Effective mass	2
1.2	Fermions-Fermi Dirac distribution, Fermi level, Doping & Energy band diagram,	2
1.3	Equilibrium and steady state conditions, Density of states & Effective density of states	1
1.4	Equilibrium concentration of electrons and holes.	1
1.5	Excess carriers in semiconductors: Generation and recombination mechanisms of excess carriers, quasi Fermi levels.	2
1.6	TUTORIAL	2
2	**MODULE 2**	
2.1	Carrier transport in semiconductors, drift, conductivity and mobility,	2

	variation of mobility with temperature and doping.	
2.2	Diffusion equation	1
2.3	Einstein relations, Poisson equations	1
2.4	Poisson equations, Continuity equations, Current flow equations	1
2.5	Diffusion length, Gradient of quasi Fermi level	1
2.6	TUTORIAL	2
3	**MODULE 3**	
3.1	PN junctions : Contact potential, Electrical Field, Potential and Charge distribution at the junction, Biasing and Energy band diagrams,	2
3.2	Ideal diode equation	1
3.3	Metal Semiconductor contacts, Electron affinity and work function, Ohmic and Rectifying Contacts, current voltage characteristics.	3
3.4	Bipolar junction transistor – working,, current components, Transistor action, Base width modulation.	2
3.5	Derivation of terminal currents in BJT	2
3.6	TUTORIAL	1
4	**MODULE 4**	
4.1	Ideal MOS capacitor, band diagrams at equilibrium, accumulation, depletion and inversion	2
4.2	Threshold voltage, body effect	1
4.3	MOSFET-structure, working, types,	2
4.4	Drain current equation (derive)- linear and saturation region, Drain characteristics, transfer characteristics.	2
4.5	TUTORIAL	1
5	**MODULE 5**	
5.1	MOSFET scaling – need for scaling, constant voltage scaling and constant field scaling.	2
5.2	Sub threshold conduction in MOS.	1
5.3	Short channel effects- Channel length modulation, Drain Induced Barrier Lowering, Velocity Saturation, Threshold Voltage Variations and Hot Carrier Effects.	3
5.4	Non-Planar MOSFETs: Fin FET –Structure, operation and advantages	1

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

MODEL QUESTION PAPER

ECT 201 SOLID STATE DEVICES

Time: 3 hours **Max. Marks:100**

PART A

Answer ***all*** questions. Each question carries ***3 marks.***

1. Draw the energy band diagram of P type and N type semiconductor materials, clearly indicating the different energy levels.
2. Indirect recombination is a slow process. Justify
3. Explain how mobility of carriers vary with temperature.
4. Show that diffusion length is the average length a carrier moves before recombination.
5. Derive the expression for contact potential in a PN junction diode.
6. Explain Early effect? Mention its effect on terminal currents of a BJT.
7. Derive the expression for threshold voltage of a MOSFET.
8. Explain the transfer characteristics of a MOSFET in linear and saturation regions.
9. Explain Subthreshold conduction in a MOSFET. Write the expression for Subthreshold current.
10. Differentiate between constant voltage scaling and constant field scaling

PART B

Answer ***any one*** question from each module. Each question carries 14 marks.

MODULE I

11. (a) Derive law of mass action. (8 marks)

(b) An n-type Si sample with $N_d = 10^5$ cm^{-3} is steadily illuminated such that $g_{op} = 10^{21}$ EHP/cm^3 s. If $\tau_n = \tau_p = 1\mu s$ for this excitation. Calculate the separation in the Quasi-Fermi levels (F_n-F_p). Draw the Energy band diagram.. (6 marks)

12. (a) Draw and explain Fermi Dirac Distribution function and position of Fermi level in intrinsic and extrinsic semiconductors. (8 marks)

(b) The Fermi level in a Silicon sample at 300 K is located at 0.3 eV below the bottom of the conduction band. The effective densities of states $N_C = 3.22 \times 10^{19}$ cm^{-3} and $N_V = 1.83 \times 10^{19}$ cm^{-3}. Determine (a) the electron and hole concentrations at 300K (b) the intrinsic carrier concentration at 400 K. (6 marks)

MODULE II

13. (a) Derive the expression for mobility, conductivity and Drift current density in a semiconductor. (8 marks)

(b) A Si bar 0.1 μm long and 100 μm^2 in cross-sectional area is doped with 10^{17} cm^{-3} phosphorus. Find the current at 300 K with 10 V applied. (b). How long will it take an average electron to drift 1 μm in pure Si at an electric field of 100 V/cm? (6 marks)

14. (a) A GaAs sample is doped so that the electron and hole drift current densities are equal in an applied electric field. Calculate the equilibrium concentration of electron and hole, the net doping and the sample resistivity at 300 K. Given μ_n = 8500 cm^2/Vs, μ_p = 400 cm^2/Vs, $n_i = 1.79 \times 10^6$ cm^{-3}. (7 marks)

(b) Derive the steady-state diffusion equations in semiconductors. (6 marks)

MODULE III

15. (a) Derive the expression for ideal diode equation. State the assumptions used. (9 marks)

(b) Boron is implanted into an n-type Si sample ($N_d = 10^{16} cm^{-3}$), forming an abrupt junction of square cross section with area = 2×10^{-3} cm^2 . Assume that the acceptor concentration in the p-type region is $N_a = 4 \times 10^{18}$ cm^{-3} . Calculate V_0 , W, Q+, and E_0 for this junction at equilibrium (300 K). (5 marks)

16. With the aid of energy band diagrams, explain how a metal – N type Schottky contact function as rectifying and ohmic contacts. (14 marks)

MODULE IV

17. (a) Starting from the fundamentals, derive the expression for drain current of a MOSFET in the two regions of operation. (8 Marks)

(b) Find the maximum depletion width, minimum capacitance C_i, and threshold voltage for an ideal MOS capacitor with a 10-nm gate oxide ($Si0_2$) on p-type Si with $N_a = 10^{16}$ cm^{-3}. (b) Include the effects of flat band voltage, assuming an n + polysilicon gate and fixed oxide charge of 5×10^{10} q (C/cm^2). (6 marks)

18. (a) Explain the CV characteristics of an ideal MOS capacitor (8 Marks)

(b) For a long channel n-MOSFET with W = 1V, calculate the V_G required for an $I_{D(sat.)}$ of 0.1 mA and $V_{D(sat.)}$ of 5V. Calculate the small-signal output conductance g and V the transconductance $g_{m(sat.)}$ at V_D = 10V. Recalculate the new I_D for (V_G - V_T) = 3 and V_D = 4V. (6 marks)

MODULE V

19. Explain Drain induced barrier lowering, Velocity Saturation, Threshold Voltage Variations and Hot Carrier Effects associated with scaling down of MOSFETs (14 marks)

20. With the aid of suitable diagrams explain the structure and working of a FINFET. List its advantages (14 marks)

ECT 203	LOGIC CIRCUIT DESIGN	CATEGORY	L	T	P	CREDIT
		PCC	3	1	0	4

Preamble: This course aims to impart the basic knowledge of logic circuits and enable students to apply it to design a digital system.

Prerequisite: EST130 Basics of Electrical and Electronics Engineering

Course Outcomes: After the completion of the course the student will be able to

CO 1	Explain the elements of digital system abstractions such as digital representations of information, digital logic and Boolean algebra
CO 2	Create an implementation of a combinational logic function described by a truth table using and/or/inv gates/ muxes
CO 3	Compare different types of logic families with respect to performance and efficiency
CO 4	Design a sequential logic circuit using the basic building blocks like flip-flops
CO 5	Design and analyze combinational and sequential logic circuits through gate level Verilog models.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	3										
CO 2	3	3	3									
CO 3	3	3										
CO 4	3	3	3									
CO 5	3	3	3		3							

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember	10	10	10
Understand	20	20	20
Apply	20	20	70
Analyse			
Evaluate			
Create			

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance	: 10 marks
Continuous Assessment Test (2 numbers)	: 25 marks
Course project	: 15 marks

It is mandatory that a *course project* shall be undertaken by a student for this subject. The course project can be performed either as a hardware realization/simulation of a typical digital system using combinational or sequential logic. Instead of two assignments, two evaluations may be performed on the course project along with series tests, each carrying 5 marks. Upon successful completion of the project, a brief report shall be submitted by the student which shall be evaluated for 5 marks. The report has to be submitted for academic auditing. A few samples projects are given below:

Sample course projects:

1. M-Sequence Generator Psuedo random sequences are popularly used in wireless communication. A sequence generator is used to produce pseudo random codes that are useful in spread spectrum applications. Their generation relies on irreducible polynomials.A maximal length sequence generator that relies on the polynomial P (D) = $D^7 + D^3 + 1$, with each D represent delay of one clock cycle.

- An 8-bit shift register that is configured as a ring counter may be used realize the above equation.
- This circuit can be developed in verilog, simulated, synthesized and programmed into a tiny FPGA and tested in real time.
- Observe the M-sequnce from parallel outputs of shift register for one period . Count the number of 1s and zeros in one cycle.
- Count the number of runs of 1s in singles, pairs, quads etc. in the pattern.

2. BCD Subtractor

- Make 4 -bit parallel adder circuit in verilog.
- Make a one digit BCD subtracter in Verilog, synthesize and write into a tiny FPGA.
- Test the circuit with BCD inputs.

3. Digital Thermometer

- Develop a circuit with a temperature sensor and discrete components to measure and dispaly temperature.
- Solder the circuit on PCB and test it.

4. Electronic Display

- This display should receive the input from an alphanumeric keyboard and display it on an LCD diplay.
- The decoder and digital circuitry is to developed in Verilog and programmed into a tiny FPGA.

5. Electronic Roulette Wheel

- 32 LEDs are placed in a circle and numbered that resembles a roulette wheel.
- A 32-bit shift register generates a random bit pattern with a single 1 in it.
- When a push button is pressed the single 1 lights one LED randomly.
- Develop the shift register random pattern generator in verilog and implement on a tiny FPGA and test the circuit.

6. Three Bit Carry Look Ahead Adder

- Design the circuit of a three bit carry look ahead adder.
- Develop the verilog code for it and implement and test it on a tiny FPGA. item Compare the performance with a parallel adder.

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks. The questions on verlog modelling should not have a credit more than 25% of the whole mark.

Course Level Assessment Questions

Course Outcome 1 (CO1) : Number Systems and Codes

1. Consider the signed binary numbers A = 01000110 and B = 11010011 where B is in 2's complement form. Find the value of the following mathematical expression (i) A + B (ii) A – B
2. Perform the following operations (i)$D9CE_{16}$-$CFDA_{16}$ (ii) 6575_8-5732_8
3. Convert decimal 6,514 to both BCD and ASCII codes. For ASCII, an even parity bit is to be appended at the left.

Course Outcome 2 (CO2) : Boolean Postulates and combinational circuits

1. Design a magnitude comparator to compare two 2-bit numbers A = A_1A_0 and B = B_1B_0B
2. Simplify using K-map F(a,b,c,d) = Σ m (4,5,7,8,9,11,12,13,15)
3. Explain the operation of a 8x1 multiplexer and implement the following using an 8x1 multiplexer F(A, B, C, D) = Σ m (0, 1, 3, 5, 6, 7, 8, 9, 11, 13, 14)

Course Outcome 3 (CO3) : Logic families and its characteristics

1. Define the terms noise margin, propagation delay and power dissipation of logic families. Compare TTL and CMOS logic families showing the values of above mentioned terms.
2. Draw the circuit and explain the operation of a TTL NAND gate
3. Compare TTL, CMOS logic families in terms of fan-in, fan-out and supply voltage

Course Outcome 4 (CO4) : Sequential Logic Circuits

1. Realize a T flip-flop using NAND gates and explain the operation with truth table, excitation table and characteristic equation
2. Explain a MOD 6 asynchronous counter using JK Flip Flop
3. Draw the logic diagram of 3 bit PIPO shift register with LOAD/SHIFT control and explain its working

Course Outcome 5 (CO5) : Logic Circuit Design using HDL

1. Design a 4-to-1 mux using gate level Verilog model.
2. Design a verilog model for a hald adder circuit. Make a one bit full adder by connecting two half adder models.
3. Compare concurrent signal assignment versus sequential signal assignment.

Syllabus

Module 1: Number Systems and Codes:

Binary and hexadecimal number systems; Methods of base conversions; Binary and hexadecimal arithmetic; Representation of signed numbers; Fixed and floating point numbers; Binary coded decimal codes; Gray codes; Excess 3 code. Alphanumeric codes: ASCII. Basics of verilog -- basic language elements: identifiers, data objects, scalar data types, operators.

Module 2: Boolean Postulates and Fundamental Gates

Boolean postulates and laws – Logic Functions and Gates De-Morgan's Theorems, Principle of Duality, Minimization of Boolean expressions, Sum of Products (SOP), Product of Sums (POS), Canonical forms, Karnaugh map Minimization. Modeling in verilog, Implementation of gates with simple verilog codes.

Module 3: Combinatorial and Arithmetic Circuits

Combinatorial Logic Systems - Comparators, Multiplexers, Demultiplexers, Encoder, Decoder. Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder. Modeling and simulation of combinatorial circuits with verilog codes at the gate level.

Module 4: Sequential Logic Circuits:

Building blocks like S-R, JK and Master-Slave JK FF, Edge triggered FF, Conversion of Flipflops, Excitation table and characteristic equation. Implementation with verilog codes. Ripple and Synchronous counters and implementation in verilog, Shift registers-SIPO, SISO, PISO, PIPO. Shift Registers with parallel Load/Shift, Ring counter and Johnsons counter. Asynchronous and Synchronous counter design, Mod N counter. Modeling and simulation of flipflops and counters in verilog.

Module 5: Logic families and its characteristics:

TTL, ECL, CMOS - Electrical characteristics of logic gates – logic levels and noise margins, fan-out, propagation delay, transition time, power consumption and power-delay product. TTL inverter - circuit description and operation; CMOS inverter - circuit description and operation; Structure and operations of TTL and CMOS gates; NAND in TTL and CMOS, NAND and NOR in CMOS.

Text Books

1. Mano M.M., Ciletti M.D., "Digital Design", Pearson India, 4th Edition. 2006
2. D.V. Hall, "Digital Circuits and Systems", Tata McGraw Hill, 1989

3. S. Brown, Z. Vranesic, “Fundamentals of Digital Logic with Verilog Design”, McGraw Hill

4. Samir Palnikar“Verilog HDL: A Guide to Digital Design and Syntheis”, Sunsoft Press

5. R.P. Jain, “Modern digital Electronics”, Tata McGraw Hill, 4th edition, 2009

Reference Books

1. W.H. Gothmann, “Digital Electronics – An introduction to theory and practice”, PHI, 2nd edition ,2006
2. Wakerly J.F., “Digital Design: Principles and Practices,” Pearson India, 4th 2008
.
3. A. Ananthakumar ,”Fundamentals of Digital Circuits”, Prentice Hall, 2nd edition, 2016
4. Fletcher, William I., An Engineering Approach to Digital Design, 1st Edition, Prentice Hall India, 1980

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**Number Systems and Codes**:	
1.1	Binary, octal and hexadecimal number systems; Methods of base conversions;	2
1.2	Binary, octal and hexadecimal arithmetic;	1
1.3	Representation of signed numbers; Fixed and floating point numbers;	3
1.4	Binary coded decimal codes; Gray codes; Excess 3 code :	1
1.5	Error detection and correction codes - parity check codes and Hamming code-Alphanumeric codes:ASCII	3
1.6	Verilog basic language elements: identifiers, data objects, scalar data types, operators	2
2	**Boolean Postulates and Fundamental Gates:**	
2.1	Boolean postulates and laws – Logic Functions and Gates, De-Morgan’s Theorems, Principle of Duality	2
2.2	Minimization of Boolean expressions, Sum of Products (SOP), Product of Sums (POS)	2
2.3	Canonical forms, Karnaugh map Minimization	1
2.4	Gate level modelling in Verilog: Basic gates, XOR using NAND and NOR	2
3	**Combinatorial and Arithmetic Circuits**	
3.1	Combinatorial Logic Systems - Comparators, Multiplexers, Demultiplexers	2
3.2	Encoder, Decoder, Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder	3

3.3	Gate level modelling combinational logic circuits in Verilog: half adder, full adder, mux, demux, decoder, encoder	3
4	**Sequential Logic Circuits:**	
4.1	Building blocks like S-R, JK and Master-Slave JK FF, Edge triggered FF	2
4.2	Conversion of Flipflops, Excitation table and characteristic equation.	1
4.3	Ripple and Synchronous counters, Shift registers-SIPO.SISO,PISO,PIPO	2
4.4	Ring counter and Johnsons counter, Asynchronous and Synchronous counter design	3
4.5	Mod N counter, Random Sequence generator	1
4.6	Modelling sequential logic circuits in Verilog: flipflops, counters	2
5	**Logic families and its characteristics**:	
5.1	TTL,ECL,CMOS- Electrical characteristics of logic gates – logic levels and noise margins, fan-out, propagation delay, transition time, power consumption and power-delay product.	3
5.2	TTL inverter - circuit description and operation	1
5.3	CMOS inverter - circuit description and operation	1
5.4	Structure and operations of TTL and CMOS gates; NAND in TTL, NAND and NOR in CMOS.	2

Simulation Assignments (ECT203)

The following simulations can be done in QUCS, KiCad or PSPICE.

BCD Adder

- Realize a one bit paraller adder, simulate and test it.
- Cascade four such adders to form a four bit parallel adder.
- Simulate it and make it into a subcircuit.
- Develop a one digit BCD adder, based on the subcircuit, simulate and test it

BCD Subtractor

- Use the above 4 -bit adder subcircuit, implement and simulate a one digit BCD subtractor.
- Test it with two BCD inputs

Logic Implementation with Multiplexer

- Develop an $8:1$ multiplexer using gates, simulate, test and make it into a subcircuit.
- Use this subcircuit to implement the logic function $f(A, B, C) = \sum m(1, 3, 7)$
- Modify the truth table properly and implement the logic function $f(A, B, C, D) = \sum m(1, 4, 12, 14)$ using one $8:1$ multiplexer.

BCD to Seven Segment Decoder

- Develop a BCD to seven segment decoder using gates and make it into a subcircuit.
- simulate this and test it

Ripple Counters

- Understand the internal circuit of 7490 IC and develop it in the simulator.
- Make it into a subcircuit and simulate it. Observe the truth table and timing diagrams for mod-5, mod-2 and mod-10 operation.
- Develop a mod-40 (mod-8 and mod-5) counter by cascading two such subcircuits.
- Simulate and observe the timing diagram and truth table.

Synchronous Counters

- Design and develop a 4-bit synchronous counter using J-K flip-flops.
- Perform digital simulation and observe the timing diagram and truth table.

Sequence Generator

- Connect D flip-flops to realize and 8-bit shift register and make it into a subcircuit.
- sequence generator that relies on the polynomial $P(D) = D_7 + D_3 + 1$, with each D represent delay of one clock cycle
- Simulate and observe this maximal length pseudo random sequence.

Transfer Characteristics of TTL and CMOS Inverters

- Develop a standard TTL circuit and perform sweep simulation and observe the transfer characteristics. Compute the threshold voltage and noise margns.
- Develop and simulate standard CMOS inverter circuit and perform sweep simulation and observe the transfer characteristics. Compute the threshold voltage and noise margins.

Model Question Paper

A P J Abdul Kalam Technological University

Third Semester B Tech Degree Examination

Branch: Electronics and Communication

Course: ECT 203 Logic Circuit Design

Time: 3 Hrs **Max. Marks: 100**

PART A

Answer All Questions

1	Convert 203.52_{10} to binary and hexadecimal.	(3)	K_1
2	Compare bitwise and logical verilog operators	(3)	K_1
3	Prove that NAND and NOR are not associative.	(3)	K_2
4	Convert the expression ABCD+AB$\overline{C}$+ACD to minterms.	(3)	K_2
5	Define expressions in Verilog with example.	(3)	K_2
6	Explain the working of a decoder.	(3)	K_1
7	What is race around condition?	(3)	K_1
8	Convert a T flip-flop to D flip-flop.	(3)	K_2
9	Define fan-in and fan-out of logic circuits.	(3)	K_2
10	Define noise margin and how can you calculate it?	(3)	K_2

PART B

Answer one question from each module. Each question carries 14 mark.

Module I

11(A)	Subtract 46_{10} from 100_{10} using 2's complement arithmetic.	(8)	K_2
11(B)	Give a brief description on keywords and identifiers in Verilog with example.	(6)	K_2

OR

12(A)	Explain the floating and fixed point representation of numbers	(8)	K_2
12(A)	Explain the differences between programming lanuguages and HDLs	(6)	K_2

Module II

13(A)	Simplify using K-map	(7)	K_3

$$f(A, B, C, D) = \sum m(4, 5, 7, 8, 9, 11, 12, 13, 15)$$

using K-maps

13(B)	Write a Verilog code for implementing above function	(7)	K_3

OR

14(A)	Write a Verilog code to implement the basic gates.	(7)	K_3
14(B)	Reduce the following Boolean function using K-Map and implement the simplified function using the logic gates	(7)	K_3

$$f(A, B, C, D) = \sum(0, 1, 4, 5, 6, 8, 9, 10, 12, 13, 14)$$

Module III

15(A)	Design a 3-bit magnitude comparator circuit.	(8)	K_3
15(B)	Write a Verilog description for a one bit full adder circuit.	(6)	K_3

OR

16(A)	Write a verilog code to implement 4:1 multiplexer	(6)	K_3
16(B)	Implement the logic function	(8)	K_3

$$f(A, B, C) = \sum m(0, 1, 4, 7)$$

using $8:1$ and $4:1$ multiplexers.

Module IV

17	Design MOD 12 asynchronous counter using T flip-flop.	(14)	K_3

OR

18(A)	Explain the operation of Master Slave JK flipflop.	(7)	K_3
18(B)	Derive the ouput Q_{n+1} in Terms of J_n, K_n and Q_n	(7)	K_3

Module V

19(A)	Explain in detail about TTL with open collector output configuration.	(8)	K_2
19(B)	Draw an ECL basic gate and explain.	(6)	K_2

OR

20(A)	Demonstrate the CMOS logic circuit configuration and characteristics in detail.	(8)	K_2
20(B)	Compare the characteristics features of TTL and ECL digital logic families	(6)	K_2

ECT205	NETWORK THEORY	CATEGORY	L	T	P	CREDIT
		PCC	3	1	0	4

Preamble: This course aims to analyze the linear time invariant electronic circuits.

Prerequisite: EST130 Basics of Electrical and Electronics Engineering

MAT102 Vector Calculus, Differential Equations and Transforms (Laplace Transform)

Course Outcomes: After the completion of the course the student will be able to

CO 1 K3	Apply Mesh / Node analysis or Network Theorems to obtain steady state response of the linear time invariant networks.
CO 2 K3	Apply Laplace Transforms to determine the transient behaviour of RLC networks.
CO 3 K3	Apply Network functions and Network Parameters to analyse the single port and two port networks.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	3										2
CO 2	3	3										2
CO 3	3	3										2

Assessment Pattern

Bloom's Category		Continuous Assessment Tests		End Semester Examination
		1	2	
Remember	K1	10	10	10
Understand	K2	20	20	20
Apply	K3	20	20	70
Analyse				
Evaluate				
Create				

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance : 10 marks

Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1): Obtain steady state response of the network using Mesh / Node analysis. (K3)

1. Enumerate different types of sources in electronic networks.

2. Solve networks containing independent and dependent sources using Mesh / Node analysis.

3. Evolve the steady-state AC analysis of a given network using Mesh or Node analysis.

Course Outcome 1 (CO1) : Obtain steady state response of the network using Network Theorems. (K3)

1. Determine the branch current of the given network with dependent source using superposition theorem.

2. State and prove Maximum Power Transfer theorem.

3. Find the Thevenin's / Norton's equivalent circuit across the port of a given network having dependent source.

Course Outcome 2 (CO2): Determine the transient behaviour of network using Laplace Transforms (K3)

1. The switch is opened at t = 0 after steady state is achieved in given network. Find the expression for the transient output current.

2. Find the Laplace Transform of a given waveform.

3. In the given circuit, the switch is closed at $t = 0$, connecting an energy source to the R,C,L circuit. At time $t = 0$, it is observed that capacitor voltage has a initial value. For the element values given, determine expression for output voltage after converting the circuit into transformed domain.

Course Outcome 3 (CO3): Apply Network functions to analyse the single port and two port network. (K3)

1. What are the necessary conditions for a network Driving point function and Transfer functions?

2. Evaluate the Driving point function and Transfer function for the given network,

3. Plot the poles and zeros of the given network.

Course Outcome 3 (CO3): Apply Network Parameters to analyse the two port network. (K3)

1. Deduce the transmission parameters of two port network in terms of two port network parameters.

2. Define the condition for a two port network to be reciprocal.

3. Two identical sections of the given networks are connected in parallel. Obtain the two port network parameters of the combination.

SYLLABUS

Module 1 : Mesh and Node Analysis

Mesh and node analysis of network containing independent and dependent sources. Supermesh and Supernode analysis. Steady-state AC analysis using Mesh and Node analysis.

Module 2 : Network Theorems

Thevenin's theorem, Norton's theorem, Superposition theorem, Reciprocity theorem, Maximum power transfer theorem. (applied to both dc and ac circuits having dependent source).

Module 3 : Application of Laplace Transforms

Review of Laplace Transforms and Inverse Laplace Transforms, Initial value theorem & Final value theorem, Transformation of basic signals and circuits into s-domain. Transient analysis of RL, RC, and RLC networks with impulse, step and sinusoidal inputs (with and without initial conditions). Analysis of networks with transformed impedance and dependent sources.

Module 4 : Network functions

Network functions for the single port and two port network. Properties of driving point and transfer functions. Significance of Poles and Zeros of network functions, Time domain response from pole zero plot. Impulse Function & Response. Network functions in the sinusoidal steady state, Magnitude and Phase response.

Module 5 : Two port network Parameters

Impedance, Admittance, Transmission and Hybrid parameters of two port network. Interrelationship among parameter sets. Series and parallel connections of two port networks. Reciprocal and Symmetrical two port network. Characteristic impedance, Image impedance and propagation constant (derivation not required).

Text Books

1. Valkenburg V., "Network Analysis", Pearson, 3/e, 2019.

2. Sudhakar A, Shyammohan S. P., "Circuits and Networks- Analysis and Synthesis", McGraw Hill, 5/e, 2015.

Reference Books

1. Edminister, "Electric Circuits – Schaum's Outline Series", McGraw-Hill, 2009.

2. W. Hayt, J. Kemmerly, J. Phillips, S. Durbin, "Engineering Circuit Analysis," McGraw Hill.

2. K. S. Suresh Kumar, "Electric Circuits and Networks", Pearson, 2008.

3. William D. Stanley, "Network Analysis with Applications", 4/e, Pearson, 2006.

4. Ravish R., "Network Analysis and Synthesis", 2/e, McGraw-Hill, 2015.

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**Mesh and Node Analysis**	
1.1	Review of circuit elements and Kirchhoff's Laws	2
1.2	Independent and dependent Sources, Source transformations	1
1.3	Mesh and node analysis of network containing independent and dependent sources	3
1.4	Supermesh and Supernode analysis	1
1.5	Steady-state AC analysis using Mesh and Node analysis	3
2	**Network Theorems (applied to both dc and ac circuits having dependent source)**	
2.1	Thevenin's theorem	1
2.2	Norton's theorem	1
2.3	Superposition theorem	2
2.4	Reciprocity theorem	1
2.5	Maximum power transfer theorem	2
3	**Application of Laplace Transforms**	
3.1	Review of Laplace Transforms	2
3.2	Initial value theorem & Final value theorem (Proof not necessary)	1
3.3	Transformation of basic signals and circuits into s-domain	2
3.4	Transient analysis of RL, RC, and RLC networks with impulse, step, pulse, exponential and sinusoidal inputs	3

3.5	Analysis of networks with transformed impedance and dependent sources	3
4	**Network functions**	
4.1	Network functions for the single port and two port network	2
4.2	Properties of driving point and transfer functions	1
4.3	Significance of Poles and Zeros of network functions, Time domain response from pole zero plot	1
4.4	Impulse Function & Response	1
4.5	Network functions in the sinusoidal steady state, Magnitude and Phase response	3
5	**Two port network Parameters**	
5.1	Impedance, Admittance, Transmission and Hybrid parameters of two port network	4
5.2	Interrelationship among parameter sets	1
5.3	Series and parallel connections of two port networks	2
5.4	Reciprocal and Symmetrical two port network	1
5.5	Characteristic impedance, Image impedance and propagation constant (derivation not required)	1

Simulation Assignments:

Atleast one assignment should be simulation of steady state and transient analysis of R, L, C circuits with different types of energy sources on any circuit simulation software. Samples of simulation assignments are listed below. The following simulations can be done in QUCS, KiCad or PSPICE.

1. Make an analytical solution of Problem 4.3 in page 113 of the book *Network Analysis* by M E Van Valkenberg. Realize this circuit in the simulator and observe *i(t)* and V_2 *(t)* using transient simulation.

2. Realize a series RLC circuit with

- R = 200Ω, L = 0.1H, C = 13.33μF
- R = 200Ω, L = 0.1H, C = 10μF and
- R = 200Ω, L = 0.1H, C = 1μF and no source respectively. The initial voltage across the capacitor is 200V Simulate the three circuits, and observe the current *i(t)* through them.

3. Repeat the above assignment for the three set of component values for a parallel RLC circuit.

4. Refer Problem 9.18 in page 208 in the book *Electric Circuits* by Nahvi and Edminister 4th Edition. See Fig. 9.28. Simulate this circuit to verify superposition theorem for the three current with individual sources and combination.

5. Refer Problem 9.22 in page 210 in the book *Electric Circuits* by Nahvi and Edminister 4th Edition. See Fig. 9.32. Implement the circuit on the simulator with V = 30$\angle$ 30°. Verify the duality between the sources V and the current *I2* and *I3* using simulation.

6. See Fig. 12.40 in Chapter 12 (page 298) in the above book. Let R1 = R2 = 2kΩ, L = 10mH and C = 40nF. Implement this circuit in the simulator and perform the ac analysis to plot the frequency response.

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, **(Model Question Paper)**

Course Code: ECT205

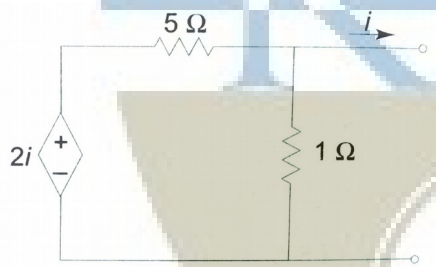
Course Name: NETWORK THEORY

Max. Marks: 100 Duration: 3 Hours

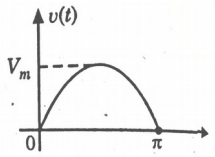
PART A

Answer ALL Questions. Each Carries 3 mark.

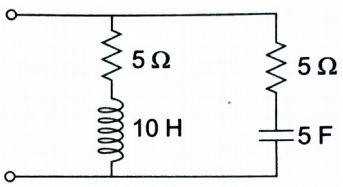
1	Illustrate the source-transformation techniques.	K2
2	Explain the concept of supernode.	K2
3	State and prove Maximum Power Transfer theorem	K1
4	Evaluate the Norton's equivalent current in the following circuit.	K3



5	Evaluate the Laplace Transform of half-wave rectified sine pulse.	K3



6	Give the two forms of transformed impedance equivalent circuit of a capacitor with initial charge across it.	K2
7	Enumerate necessary condition for a Network Functions to be Transfer Functions.	K1
8	Obtain the pole zero configuration of the impedance function of the following circuit.	K3



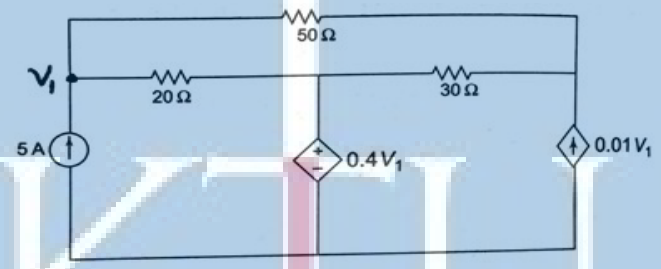
9	Define the short-circuit admittance parameter with its equivalent circuit.	K2
10	Deduce Z-parameter in terms of h-parameter.	K2

PART – B

Answer one question from each module; each question carries 14 marks.

Module - I

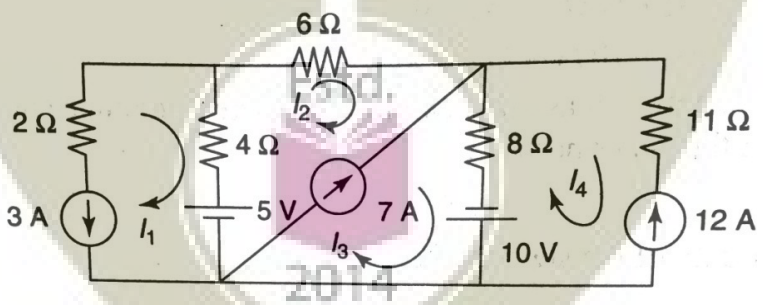
11 a.	Find the voltage V_1 using nodal analysis.	7



CO1

K3

b.	Find the current through 8 ohms resistor in the following circuit using mesh analysis.	7



CO1

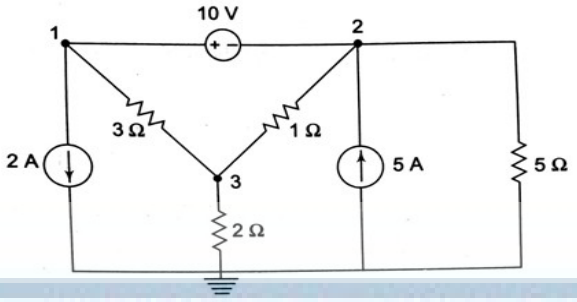
K3

OR

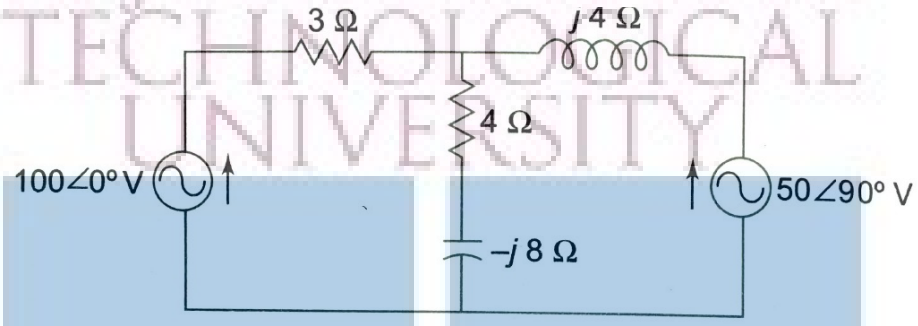
12	Find the power delivered by the 5A current source using nodal analysis method.	7

CO1

K3

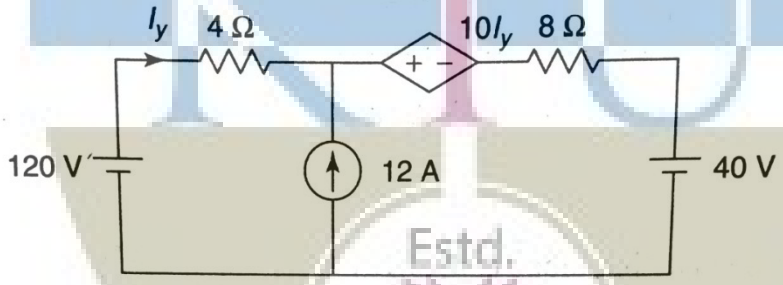


b. Determine the values of source currents using Mesh analysis 7 CO1 K3

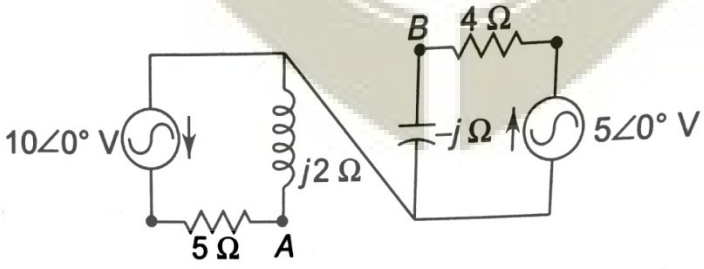


Module - II

13 a. Find the current I_y by superposition principle. 7 CO1 K3

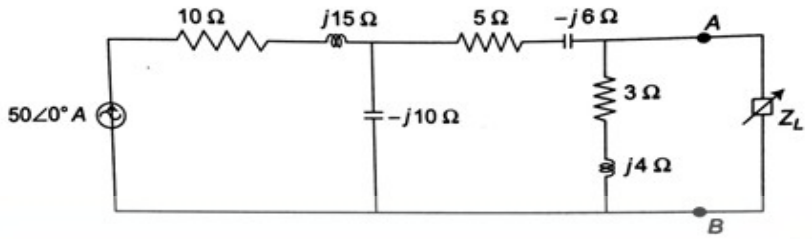


b. Find the Norton's equivalent circuit across the port **AB**. 7 CO1 K3



OR

14 Determine the maximum power delivered to the load in the circuit. 14



CO1

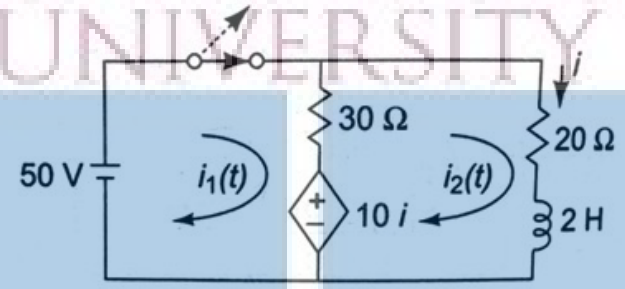
K3

Module - III

15 a. The switch is opened at t = 0 after steady state is achieved. Find the expression for the transient current ***i***. 8

CO2

K3



b. A voltage pulse of unit height and width ' ***T*** ' is applied to a low pass RC circuit at time t=0. Determine the expression for the voltage across the capacitor C as a function of time. 6

CO2

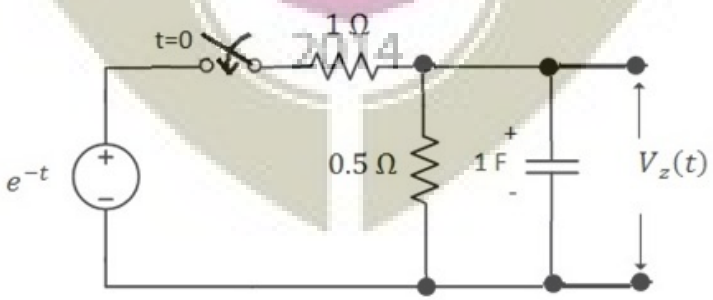
K3

OR

16 In the circuit, the switch is closed at $t = 0$, connecting a source e^{-t} to the RC circuit. At time $t = 0$, it is observed that capacitor voltage has the value $V_c(0) = 0.5V$. For the element values given, determine $V_z(t)$ after converting the circuit into transformed domain. 14

CO2

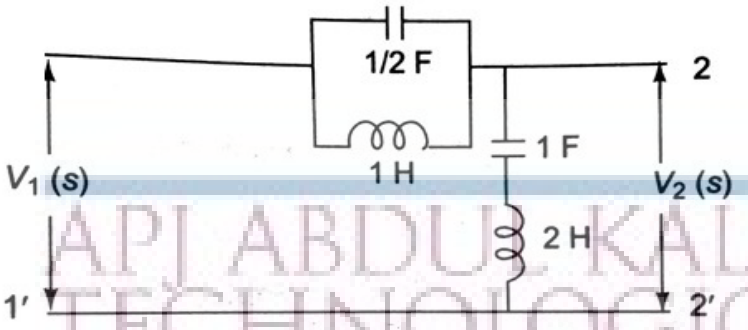
K3



Module - IV

17 For the network, determine Driving point impedance $Z_{11}(s)$, Voltage gain Transfer 14

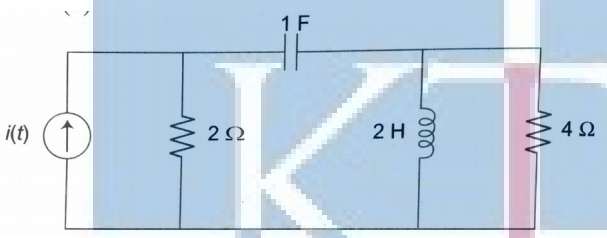
function $G_{21}(s)$ and Current gain Transfer function $\alpha_{21}(s)$. CO3 K3



OR

18 a. Compare and contrast the necessary conditions for a network Driving point function and Transfer functions. 7 CO3 K2

b. For following network, evaluate the admittance function Y(s) as seen by the source i(t). Also pot the poles and zeros of Y(s). 7 CO3 K3



Module - V

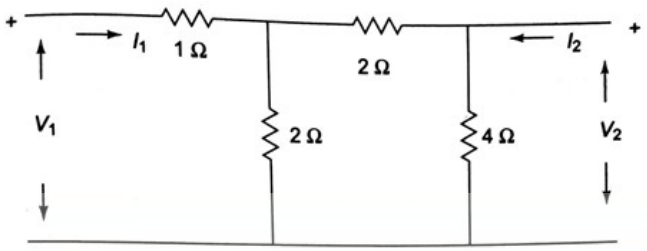
19 a. Deduce the transmission parameters of two port network in terms of 10 CO4 K2

(i) Z-parameters, (ii) Y-parameters and (iii) Hybrid parameters.

b. How to determine the given two port network is Symmetrical 4 K2

OR

20 Two identical sections of the following networks are connected in parallel. Obtain the Y-parameters of the combination. 14 K3



ECL 201	SCIENTIFIC COMPUTING LABORATORY	CATEGORY	L	T	P	CREDIT
		PCC	0	0	3	2

Preamble

- The following experiments are designed to translate the mathematical concepts into system design.
- The students shall use Python for realization of experiments. Other softwares such as R/MATLAB/SCILAB/LabVIEW can also be used.
- The experiments will lay the foundation for future labs such as DSP lab.
- The first two experiments are mandatory and any six of the rest should be done.

Prerequisites

- MAT 101 Linear Algebra and Calculus
- MAT 102 Vector Calculus, Differential Equations and Transforms

Course Outcomes The student will be able to

CO 1	Describe the needs and requirements of scientific computing and to familiarize one programming language for scientific computing and data visualization.
CO 2	Approximate an array/matrix with matrix decomposition.
CO 3	Implement numerical integration and differentiation.
CO 4	Solve ordinary differential equations for engineering applications
CO 5	Compute with exported data from instruments
CO 6	Realize how periodic functions are constituted by sinusoids
CO 7	Simulate random processes and understand their statistics.

Mapping of Course Outcomes with Program Outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	3	0	0	0	3	1	0	3
CO2	3	3	1	2	3	0	0	0	3	0	0	1
CO3	3	3	1	1	3	0	0	0	0	0	0	1
CO4	3	3	1	1	3	0	0	0	0	0	0	1
CO5	3	3	1	3	0	0	0	0	3	3	0	0
CO6	3	3	2	2	3	0	0	0	3	1	0	0
CO7	3	3	2	2	3	0	0	0	3	1	0	1

Assessment Pattern

Mark Distribution

Total Mark	CIE	ESE
150	75	75

Continuous Internal Evaluation Pattern

Attribute	Mark
Attendance	15
Continuous assessment	30
Internal Test (Immediately before the second series test)	30

End Semester Examination Pattern The following guidelines should be followed regarding award of marks.

Attribute	Mark
Preliminary work	15
Implementing the work/Conducting the experiment	10
Performance, result and inference (usage of equipments and trouble shooting)	25
Viva voce	20
Record	5

General instructions: End-semester practical examination is to be conducted immediately after the second series test covering entire syllabus given below. Evaluation is to be conducted under the equal responsibility of both the internal and external examiners. The number of candidates evaluated per day should not exceed 20. Students shall be allowed for the examination only on submitting the duly certified record. The external examiner shall endorse the record.

Course Level Assessment Questions

CO1-The needs and requirements of scientific computing and to familiarize one programming language for scientific computing and data visualization

1. Write a function to compute the first N Fibonacci numbers. Run this code and test it.
2. Write a function to compute the sum of N complex numbers. Run this code and test it.
3. Write a function to compute the factorial of an integer. Run this code and test it.

CO2-Approximation an array/matrix with matrix decomposition.

1. Write a function to compute the eigen values of a real valed valued matrix (say 5×5). Run this code. Plot the eigen values and understand their variation.
2. Write a function to approximate a 5×5 matrix using its first 3 eigen vales. Run the code and compute the absolute square error in the approximation.

CO3-Numerical Integration and Differentiation

1. Write and execute a function to return the first and second derivative of the function $f(t) = 3t^4 + 5$ for the vector $t = [-3, 3]$.
2. Write and execute a function to return the value of

$$\int_{-3}^{3} e^{-|t|}\, dt$$

CO4-Solution of ODE

1. Write and execute a function to return the numerical solution of

$$\frac{d^2x}{dt^2} + 4\frac{dx}{dt} + 2x = e^{-t}\cos(t)$$

.

2. Write and execute a function to solve for the current transient through an RL network (with $\frac{r}{L} = 1$) that is driven by the signal $5e^{-t}U(t)$

CO5-Data Analysis

1. Connect a signal generator toa DSO and display a $1\,V$, $3\,kHz$ signal. Store the trace in a usb device as a spreadsheet. Write and execute a function to load and dispaly signal from the spreadsheet. Compute the rms value of the signal.
2. Write and execute a program to display random data in two dimensions as continuous and discrete plots.

CO6-Convergence of Fourier Series

1. Write the Fourier series of a traingular signal. Compute this sum for 10 and 50 terms respectively. Plot both signals on the same GUI.

CO7-Simulation of Random Phenomena

1. Write and execute a function to toss three fair coins simultaneously. Compute the probability of getting exactly two heads for 100 and 1000 number of tosses

Experiments

Experiment 1. Familarization of the Computing Tool

1. Needs and requirements in scientific computing
2. Familiarization of a programming language like Python/R/ MATLAB/SCILAB/LabVIEW for scientific computing
3. Familiarization of data types in the language used.
4. Familiarization of the syntax of *while*, *for*, *if* statements.
5. Basic syntax and execution of small scripts.

Experiment 2. Familarization of Scientific Computing

1. Functions with examples
2. Basic arithmetic functions such as *abs*, *sine*, *real*, *imag*, *complex*, *sinc* etc. using bulit in modules.
3. Vectorized computing without loops for fast scientific applications.

Experiment 3. Realization of Arrays and Matrices

1. Realize one dimensional array of real and complex numbers
2. stem and continous plots of real arrays using *matplotlib*/GUIs/charts.
3. Realization of two dimensional arrays and matrices and their visualizations with *imshow/matshow/charts*
4. Inverse of a square matrix and the solution of the matrix equation

$$[\mathbf{A}][\mathbf{X}] = [\mathbf{b}]$$

where $\mathbf{A}$ is an $N \times N$ matrix and $\mathbf{X}$ and $\mathbf{b}$ are $N \times 1$ vectors.

5. Computation of the rank(ρ) and eigen values (λ_i) of $\mathbf{A}$
6. Approximate $\mathbf{A}$ for $N = 1000$ with the help of singular value decomposition of $\mathbf{A}$ as

$$\tilde{\mathbf{A}} = \sum_{i=0}^{r} \lambda_i U_i V_i^T$$

where U_i and V_i are the singular vectors and λ_i are the eigen values with $\lambda_i < \lambda_j$ for $i > j$. One may use the built-in functions for singular value decomposition.

7. Plot the absolute error(ζ) between $\mathbf{A}$ and $\tilde{\mathbf{A}}$ as $\zeta = \sum_{i=1}^{N} \sum_{j=1}^{N} |a_{i,j} - \tilde{a_{i,j}}|^2$ against r for $r = 10, 50, 75, 100, 250\ , 500, 750$ and appreciate the plot.

Experiment 4. Numerical Differentiation and Integration

1. Realize the functions $\sin t$, $\cos t$, *sinht* and *cosht* for the vector $t = [0, 10]$ with increment 0.01
2. Compute the first and second derivatives of these functions using built in tools such as *grad*.
3. Plot the derivatives over the respective functions and appreciate.
4. Familiarize the numerical integration tools in the language you use.
5. Realize the function

$$f(t) = 4t^2 + 3$$

and plot it for the vector $t = [-5, 5]$ with increment 0.01

6. Use general integration tool to compute

$$\int_{-2}^{2} f(t)\,dt$$

7. Repeat the above steps with trapezoidal and Simpson method and compare the results.
8. Compute

$$\frac{1}{\sqrt{2\pi}}\int_{0}^{\infty} e^{-\frac{x^2}{2}}\,dx$$

using the above three methods.

Experiment 5. Solution of Ordinary Differential Equations

1. Solve the first order differential equation

$$\frac{dx}{dt} + 2x = 0$$

with the initial condition $x(0) = 1$

2. Solve for the current transient through an RC network (with $RC = 3$) that is driven by
   - $5\,V$ DC
   - the signal $5e^{-t}U(t)$

   and plot the solutions.
3. Solve the second order differential equation

$$\frac{d^2x}{dt^2} + 2\frac{dx}{dt} + 2x = e^{-t}$$

4. Solve the current transient through a series RLC circuit with $R = 1\Omega$, $L = 1\,mH$ and $C = 1\,\mu F$ that is driven by
   - $5\,V$ DC
   - the signal $5e^{-t}U(t)$

Experiment 6. Simple Data Visualization

1. Draw stem plots, line plots, box plots, bar plots and scatter plots with random data.
2. plot the histogram of a random data.
3. create legends in plots.
4. Realize a vector $t = [-10, 10]$ with increment 0.01 as an array.
5. Implement and plot the functions
   - $f(t) = \cos t$
   - $f(t) = \cos t \cos 5t + \cos 5t$

Experiment 7. Simple Data Analysis with Spreadsheets

1. Display an electrical signal on DSO and export it as a *.csv* file.
2. Read this *.csv* or *.xls* file as an array and plot it.
3. Compute the mean and standard deviation of the signal. Plot its histogram with an appropriate bin size.

Experiment 8. Convergence of Fourier Series

1. The experiment aims to understand the lack of convergence of Fourier series
2. Realize the Fourier series
$$f(t) = \frac{4}{\pi}[1 - \frac{1}{3}\cos\frac{2\pi 3t}{T} + \frac{1}{5}\cos\frac{2\pi 5t}{T} - \frac{1}{7}\cos\frac{2\pi 7t}{T} + \cdots]$$
3. Realize the vector $t = [0, 100]$ with an increment of 0.01 and keep $T = 20$.
4. Plot the first 3 or 4 terms on the same graphic window and understand how the smooth sinusoids add up to a discontinous square function.
5. Compute and plot the series for the first 10, 20, 50 and 100 terms of the and understand the lack of convergence at the points of discontinuity.
6. With t made a zero vector, $f(0) = 1$, resulting in the *Madhava* series for π as
$$\pi = 4[1 - \frac{1}{3} + \frac{1}{5} - \frac{1}{7} + \cdots]$$
7. Use this to compute π for the first 10, 20, 50 and 100 terms.

Experiment 9: Coin Toss and the Level Crossing Problem

1. Simulate a coin toss that maps a head as 1 and tail as 0.
2. Toss the coin $N = 100$, 500,1000, 5000 and 500000 times and compute the probability (p) of head in each case.
3. Compute the absolute error $|0.5 - p|$ in each case and plot against N and understand the law of large numbers.
4. Create a uniform random vector with maximum magnitude 10, plot and observe.
5. Set a threshold ($V_T = 2$) and count how many times the random function has crossed V_T.
6. Count how many times the function has gone above and below the threshold.

Schedule of Experiments Every experiment should be completed in three hours.

ECL 203	LOGIC DESIGN LAB	CATEGORY	L	T	P	CREDIT
		PCC	0	0	3	2

Preamble: This course aims to (i) familiarize students with the Digital Logic Design through the implementation of Logic Circuits using ICs of basic logic gates (ii) familiarize students with the HDL based Digital Design Flow.

Prerequisite: Nil

Course Outcomes: After the completion of the course the student will be able to

CO 1	Design and demonstrate the functioning of various combinational and sequential circuits using ICs
CO 2	Apply an industry compatible hardware description language to implement digital circuits
CO 3	Implement digital circuis on FPGA boards and connect external hardware to the boards
CO 4	Function effectively as an individual and in a team to accomplish the given task

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	3	3						3			3
CO 2	3	1	1	3	3				3			3
CO 3	3	1	1	3	3				3	1		3
CO 4	3	3	3		3				3			3

Assessment

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	75	75	2.5 hours

Continuous Internal Evaluation Pattern:

Attendance : 15 marks
Continuous Assessment : 30 marks

Internal Test (Immediately before the second series test) : 30 marks

End Semester Examination Pattern: The following guidelines should be followed regarding award of marks

(a) Preliminary work : 15 Marks
(b) Implementing the work/Conducting the experiment : 10 Marks
(c) Performance, result and inference (usage of equipments and trouble shooting) : 25 Marks
(d) Viva voce : 20 marks
(e) Record : 5 Marks

General instructions: End-semester practical examination is to be conducted immediately after the second series test covering entire syllabus given below. Evaluation is to be conducted under the equal responsibility of both the internal and external examiners. The number of candidates evaluated per day should not exceed 20. Students shall be allowed for the examination only on submitting the duly certified record. The external examiner shall endorse the record.

Course Level Assessment Questions

Course Outcome 1 (CO1): Design and Development of combinational circuits

1. Design a one bit full adder using gates and implement and test it on board.

2. Implement and test the logic function f(A,B,C)=∑m(0,1,3,6) using an 8:1 Mux IC

3. Convert a D flip-flop to T flip-flop and implement and test on board.

Course Outcome 2 and 3 (CO2 and CO3): Implementation of logic circuits on tiny FPGA

1. Design and implement a one bit subtracter in Verilog and implement and test it on a tiny FPGA board.

2. Design and implement a J-K flip-flop in Verilog, implement and test it on a tiny FPGA board.

3. Design a 4:1 Multiplexer in Verilog and implement and test it on tiny FPGA board.

List of Experiments:

It is compulsory to conduct a minimum of 5 experiments from Part A and a minimum of 5 experiments from Part B.

Part A (Any 5)

The following experiements can be conducted on breadboard or trainer kits.

1. Realization of functions using basic and universal gates (SOP and POS forms).
2. Design and Realization of half /full adder and subtractor using basic gates and universal gates.
3. 4 bit adder/subtractor and BCD adder using 7483.
4. Study of Flip Flops: S-R, D, T, JK and Master Slave JK FF using NAND gates.
5. Asynchronous Counter:3 bit up/down counter

6. Asynchronous Counter:Realization of Mod N counter
7. Synchronous Counter: Realization of 4-bit up/down counter.
8. Synchronous Counter: Realization of Mod-N counters.
9. Ring counter and Johnson Counter. (using FF & 7495).
10. Realization of counters using IC's (7490, 7492, 7493).
11. Multiplexers and De-multiplexers using gates and ICs. (74150, 74154)
12. Realization of combinational circuits using MUX & DEMUX.
13. Random Sequence generator using LFSR.

PART B (Any 5)

The following experiments aim at training the students in digital circuit design with verilog and implementation in small FPGAs. Small, low cost FPGAs, that can be driven by open tools for simulation, synthesis and place and route, such as *TinyFPGA* or *Lattice iCEstick* can be used. Open software tools such as *yosis* (for simulation and synthesis) and *arachne* (for place and route) may be used. The experiments will lay the foundation for digital design with FPGA with the objective of increased employability.

Experiment 1. Realization of Logic Gates and Familiarization of FPGAs

(a) Familiarization of a small FPGA bboard and its ports and interface.
(b) Create the .pcf files for your FPGA board.
(c) Familiarization of the basic syntax of verilog
(d) Development of verilog modules for basic gates, synthesis and implementation in the above FPGA to verify the truth tables.
(e) Verify the universality and non associativity of NAND and NOR gates by uploading the corresponding verilog files to the FPGA boards.

Experiement 2: Adders in Verilog

(a) Development of verilog modules for half adder in 3 modeling styles (dataflow/structural/ behavioural).
(b) Development of verilog modules for full adder in structural modeling using half adder.

Experiement 3: Mux and Demux in Verilog

(a) Development of verilog modules for a 4x1 MUX.
(b) Development of verilog modules for a 1x4 DEMUX.

Experiement 4: Flipflops and coutners

(a) Development of verilog modules for SR, JK and D flipflops.
(b) Development of verilog modules for a binary decade/Johnson/Ring counters

Experiment 5. Multiplexer and Logic Implementation in FPGA

(a) Make a gate level design of an 8 : 1 multiplexer, write to FPGA and test its functionality.
(b) Use the above module to realize the logic function f (A, B, C) = ∑m(0, 1, 3, 7) and test it.
(c) Use the same 8 : 1 multiplexer to realize the logic function f (A, B, C, D) = ∑m(0, 1, 3, 7, 10, 12) by partitioning the truth table properly and test it.

Experiment 6. Flip-Flops and their Conversion in FPGA

(a) Make gate level designs of J-K, J-K master-slave, T and D flip-flops, implement and test them on the FPGA board.
(b) Implement and test the conversions such as T to D, D to T, J-K to T and J-K to D

Experiment 7: Asynchronous and Synchronous Counters in FPGA

(a) Make a design of a 4-bit up down ripple counter using T-flip-lops in the previous experiment, implement and test them on the FPGA board.
(b) Make a design of a 4-bit up down synchronous counter using T-flip-lops in the previous experiment, implement and test them on the FPGAboard.

Experiment 8: Universal Shift Register in FPGA

(a) Make a design of a 4-bit universal shift register using D-flip-flops in the previous experiment, implement and test them on the FPGA board.
(b) Implement ring and Johnson counters with it.

Experiment 9. BCD to Seven Segment Decoder in FPGA

(a) Make a gate level design of a seven segment decoder, write to FPGA and test its functionality.
(b) Test it with switches and seven segment display. Use ouput ports for connection to the display.

SEMESTER -3

MINOR

ECT281	ELECTRONIC CIRCUITS	CATEGORY	L	T	P	CREDIT
		Minor	3	1	0	4

Preamble: This course aims to develop the skill of the design of various analog circuits.

Prerequisite: EST130 Basics of Electrical and Electronics Engineering

Course Outcomes: After the completion of the course the student will be able to

CO 1	Realize simple circuits using diodes, resistors and capacitors
CO 2	Design amplifier and oscillator circuits
CO 3	Design Power supplies, D/A and A/D convertors for various applications
CO4	Design and analyze circuits using operational amplifiers

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	3										2
CO 2	3	3										2
CO 3	3	3										2
CO 4	3	3										2

Assessment Pattern

Bloom's Category		Continuous Assessment Tests		End Semester Examination
		1	2	
Remember	K1	10	10	10
Understand	K2	20	20	20
Apply	K3	20	20	70
Analyse	K4			
Evaluate				
Create				

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1): Realize simple circuits using diodes, resistors and capacitors.

1. For the given specification design a differentiator and integrator circuit.
2. For the given input waveform and circuit, draw the output waveform and transfer characteristics.
3. Explain the working of RC differentiator and integrator circuits and sketch the output waveform for different time periods.

Course Outcome 2 (CO2): Design amplifier and oscillator circuits.

1. For the given transistor biasing circuit, determine the resistor values, biasing currents and voltages.
2. Explain the construction, principle of operation, and characteristics of MOSFETs.
3. Design a RC coupled amplifier for a given gain.
4. Design a Hartley oscillator to generate a given frequency.

Course Outcome 3 (CO3): Design Power supplies, D/A and A/D convertors for various applications.

1. Design a series voltage regulator.
2. For the regulator circuit, find the output voltage and current through the zener diode.
3. In a 10 bit DAC, for a given reference voltage, find the analog output for the given digital input.

Course Outcome 4 (CO4): Design circuits using operational amplifiers for various applications

1. For the given difference amplifier, find the output voltage.
2. Derive the expression for frequency of oscillation of Wien bridge oscillator using op-amp.
3. Realize a summing amplifier to obtain a given output voltage.

SYLLABUS

Module 1:

Wave shaping circuits: Sinusoidal and non-sinusoidal wave shapes, Principle and working of RC differentiating and integrating circuits, Clipping circuits - Positive, negative and biased clipper. Clamping circuits - Positive, negative and biased clamper.

Transistor biasing: Introduction, operating point, concept of load line, thermal stability (derivation not required), fixed bias, self bias, voltage divider bias.

Module 2:

MOSFET- Structure, Enhancement and Depletion types, principle of operation and characteristics.

Amplifiers: Classification of amplifiers, RC coupled amplifier – design and working, voltage gain and frequency response. Multistage amplifiers - effect of cascading on gain and bandwidth.

Feedback in amplifiers - Effect of negative feedback on amplifiers.

MOSFET Amplifier- Circuit diagram, design and working of common source MOSFET amplifier.

Module 3:

Oscillators: Classification, criterion for oscillation, Wien bridge oscillator, Hartley and Crystal oscillator. (design equations and working of the circuits; analysis not required).

Regulated power supplies: Review of simple zener voltage regulator, series voltage regulator, 3 pin regulators-78XX and 79XX, DC to DC conversion, Circuit/block diagram and working of SMPS.

Module 4 : Operational amplifiers: Characteristics of op-amps(gain, bandwidth, slew rate, CMRR, offset voltage, offset current), comparison of ideal and practical op-amp(IC741), applications of op-amps- scale changer, sign changer, adder/summing amplifier, subtractor, integrator, differentiator, Comparator, Instrumentation amplifier.

Module 5:

Integrated circuits: D/A and A/D convertors – important specifications, Sample and hold circuit, R-2R ladder type D/A convertors.

Flash and sigma-delta type A/D convertors.

Text Books

1. Robert Boylestad and L Nashelsky, Electronic Devices and Circuit Theory, Pearson, 2015.
2. Salivahanan S. and V. S. K. Bhaaskaran, Linear Integrated Circuits, Tata McGraw Hill, 2008.

Reference Books

1. David A Bell, Electronic Devices and Circuits, Oxford University Press, 2008.

2. Neamen D., Electronic Circuits, Analysis and Design, 3/e, TMH, 2007.

3. Millman J. and C. Halkias, Integrated Electronics, 2/e, McGraw-Hill, 2010.

4. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, PHI, 2000.

5. K.Gopakumar, Design and Analysis of Electronic Circuits, Phasor Books, Kollam, 2013

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**Wave shaping circuits**	
1.1	Sinusoidal and non-sinusoidal wave shapes	1
1.2	Principle and working of RC differentiating and integrating circuits	2
1.3	Clipping circuits - Positive, negative and biased clipper	1
1.4	Clamping circuits - Positive, negative and biased clamper	1
	Transistor biasing	
1.5	Introduction, operating point, concept of load line	1
	Thermal stability, fixed bias, self bias, voltage divider bias.	3
2	**Field effect transistors**	
2.2	MOSFET- Structure, Enhancement and Depletion types, principle of operation and characteristics	2
	Amplifiers	
2.3	Classification of amplifiers, RC coupled amplifier - design and working voltage gain and frequency response	3
2.4	Multistage amplifiers - effect of cascading on gain and bandwidth	1
2.5	Feedback in amplifiers - Effect of negative feedback on amplifiers	1
	MOSFET Amplifier- Circuit diagram, design and working of common source MOSFET amplifier	2
3	**Oscillators**	
3.1	Classification, criterion for oscillation	1
3.2	Wien bridge oscillator, Hartley and Crystal oscillator	3
	Regulated power supplies	
3.3	simple zener voltage regulator, series voltage regulator line and load regulation	3
3.4	3 pin regulators-78XX and 79XX	1
3.5	DC to DC conversion, Circuit/block diagram and working of SMPS	1
4	**Operational amplifiers**	
4.1	Differential amplifier	2
4.2	characteristics of op-amps(gain, bandwidth, slew rate, CMRR, offset voltage, offset current), comparison of ideal and practical op-amp(IC741)	2
4.3	applications of op-amps- scale changer, sign changer, adder/summing amplifier, subtractor, integrator, differentiator	3

4.4	Comparator, Schmitt trigger, Linear sweep generator	3
5	**Integrated circuits**	
5.1	D/A and A/D convertors – important specifications, Sample and hold circuit	1
5.2	R-2R ladder type D/A convertors	2
5.3	Flash and successive approximation type A/D convertors	2
5.4	Circuit diagram and working of Timer IC555, astable and monostable multivibrators using 555	3

Assignment:

Atleast one assignment should be simulation of transistor amplifiers and op-amps on any circuit simulation software.

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, (**Model Question Paper)**

Course Code: ECT281

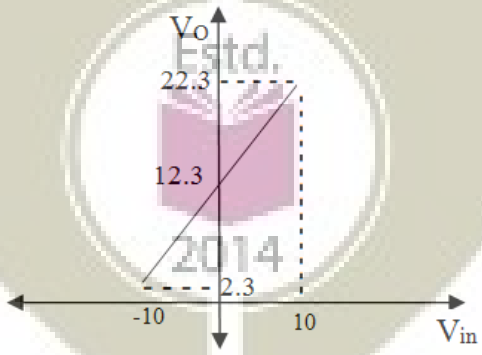
Course Name: ELECTRONIC CIRCUITS

Max. Marks: 100 Duration: 3 Hours

PART A

Answer ALL Questions. Each Carries 3 mark.

1 Design a clamper circuit to get the following transfer characteristics, assuming voltage drop across the diode s 0.7V. K3



2 Give the importance of biasing in transistors? Mention significance of operating point. K2

3 What is line regulation and load regulation in the context of a voltage regulator? Explain with equation for percentage of regulation:- K2

4 Compare the features of FET with BJT:- K1

5 What is the effect of cascading in gain and bandwidth of amplifier? K1

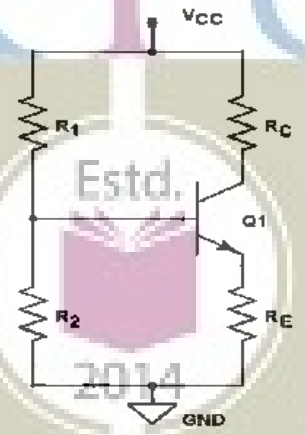
6	Discuss about simple zener shunt voltage regulator:-	K1
7	Realize a circuit to obtain Vo= $-2V_1+3V_2+4V_3$ using operational amplifier. Use minimum value of resistance as 10KΩ.	K3
8	Design a monostable multivibrator using IC 555 timer for a pulse period of 1 ms.	K3
9	Describe the working of a Flash type A/D Converter, with example.	K2
10	Define: (1) Slew rate, (2) CMRR, (3) offset voltage and current:-	K2

PART – B

Answer one question from each module; each question carries 14 marks.

Module - I

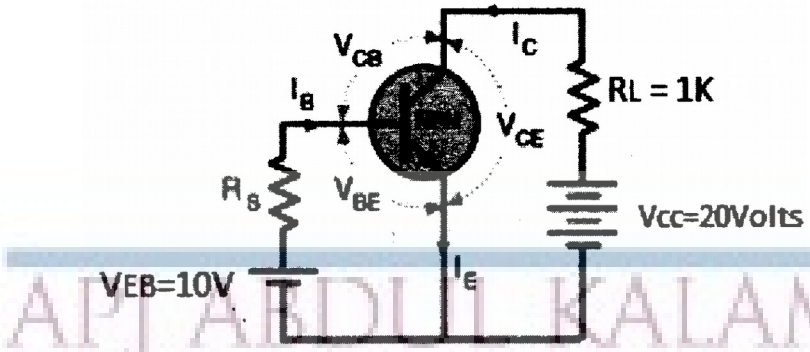
11 a.	Design a differentiator circuit for a square wave signal with Vpp=10 and frequency 10KHz:-	5	CO1 K3
b.	Consider a self-biasing circuit shown in figure below with Vcc=20V, R_c=1.5KΩ, which is operated at Q-point (Vce=8V, Ic=4mA), If h_{FE}=100, find R_1, R_2 and R_e. Assume V_{BE}=0.7V.	9	CO2 K3



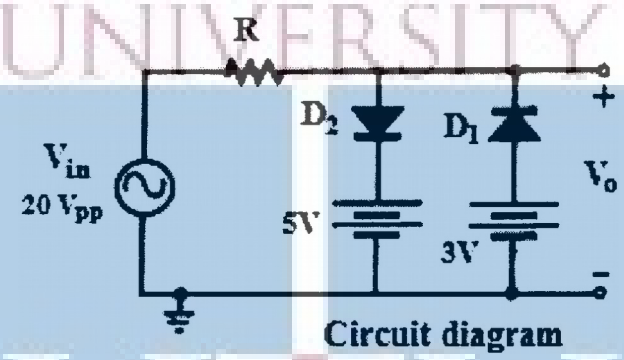
OR

12 a.	Explain the working of an RC differentiator circuit for a square wave input with period T.Sketchits output waveform for RC ≫ T ,RC ≪ T and RC = T.	5	CO1 K3
b.	With reference to the following circuit, draw the load line and mark the Q point of a Silicon transistor operating in CE mode based on the following data (β=80, Rs=47KΩ, R_L=1KΩ, neglect I_{CBO})	5	CO2

K3



c. Draw the output waveform and transfer characteristics of the given clipper circuit. 4 CO1 K3



Circuit diagram

Module - II

13 a. With neat sketches, explain the construction, principle of operation and characteristics of an N-channel enhancement MOSFET:- 9 CO2 K2

b. Draw the circuit of an RC coupled amplifier and explain the function of each element:- 5 CO2 K2

OR

14 a. Draw the circuit of a common source amplifier using MOSFET. Derive the expressions for voltage gain and input resistance:- 9 CO2 K2

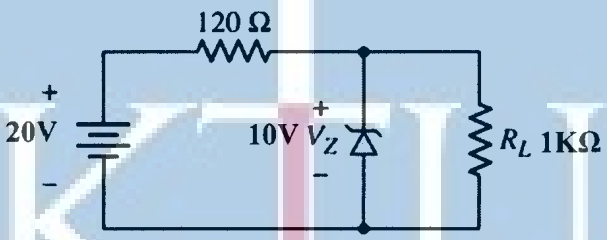
b. Sketch the frequency response of an RC coupled amplifier and write the reasons for gain reduction in both ends. 5 CO2 K2

Module - III

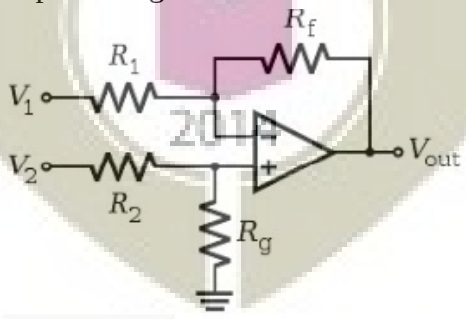
15 a. Design a Hartley oscillator to generate a frequency of 150KHz. 5 CO2

			K3
b.	Draw the circuit of a series voltage regulator. Explain its working when the input voltage as well as load current varies. Design a circuit to deliver 5V, 100mA maximum load current:-	9	CO3 K3

OR

16 a.	With neat diagram and relevant equations explain the working of wein bridge oscillator using BJT:-	7	CO2 K2
b.	Derive the expression for the frequency of oscillation of Wien bridge oscillator using BJT	4	CO2 K2
c.	For the circuit shown below, find the ouput voltage across RL and current through the zener diode:- 	3	CO3 K3

Module - IV

17 a.	With circuit, relevant equations and waveforms explain the working of a Schmit trigger using op-amp:-	10	CO4 K2
b.	The difference amplifier shown in the figure have R_1=R_2=5KΩ, R_F=10KΩ, R_g=1KΩ. Calculate the output voltage. 	5	CO4 K3

OR

18 a.	With circuits and equations show that an op-amp can act as integrator, differentiator, adder and subtractor.	9	CO4 K2

b.	What do you mean by differential amplifier? With neat sketches, explain the working of an open loop OP-AMP differential amplifier.	5	CO4 K2

Module - V

19 a.	Explain the working of R-2R ladder type DAC. In a 10 bit DAC, reference voltage is given as 15V. Find analog output for digital input of 1011011001.	10	CO3 K3
b.	With neat diagram explain the working of IC555 timer.	4	CO4 K3

OR

20 a.	A 4-bit R-2R ladder type DAC having R= 10 kΩ and V_R= 10 V. Find its resolution and output voltage for an input 1101.	4	CO4 K3
b.	Design an astable multivibrator using IC 555 timer for a frequency of 1KHz and a duty cycle of 70%.Assume c=0.1μF.	5	CO4 K3
c.	Draw the circuit diagram of a simple sample and hold circuit and explain the necessity of this circuit in A to D conversion.	5	CO4 K2

Simulation Assignments

The following simulations can be done in QUCS, KiCad or PSPICE.

1. Design and simulate RC coupled amplifer. Observe the input and output signals. Plot the AC frequency response and understand the variation of gain at high frequencies. Observe the effect of negative feedback by changing the capacitor across the emitter resistor.
2. Design and simulate Wien bridge oscillator for a frequency of $10\,kHz$. Run a transient simulation and observe the output waveform.
3. Design and simulate series voltage regulator for output voltage $V_O = 10V$ and output current $I_O = 100mA$ with and without short circuit protection and to test the line and load regulations.
4. Design and implement differential amplifier and measure its CMRR. Plot its transfer characteristics.
5. Design and simulate non-inverting amplifier for gain 5. Observe the input and output signals. Run the ac simulation and observe the frequency response and $3-$ db bandwidth.
6. Design and simulate a 3 bit flash type ADC. Observe the output bit patterns and transfer characteristics
7. Design and simulate $R-2R$ DAC ciruit.
8. Design and implement Schmitt trigger circuit for upper triggering point of $+8\,V$ and a lower triggering point of $-4\,V$ using op-amps.

ECT 283	ANALOG COMMUNICATION	CATEGORY	L	T	P	CREDIT
		Minor	3	1	0	4

Preamble: The course has two objectives: (1) to study two analog modulation schemes known as amplitude modulation and frequency modulation (2) to understand the implementations of transmitter and reciever systems used in AM and FM.

Prerequisite: NIL

Course Outcomes: After the completion of the course the student will be able to

CO 1	Explain various components of a communication system
CO 2	Discuss various sources of noise, and its the effect in a communication system
CO 3	Explain amplitude modulation and its variants for a sinusoidal message
CO 4	Explain frequency modulation and its variants for a sinusoidal message
CO 5	List and compare various transmitter and receiver systems of AM and FM

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	3										
CO 2	3	3										
CO 3	3	3										
CO 4	3	3										
CO 5	3	3										
CO 6	3	3										

Assessment Pattern

Bloom's Category		Continuous Assessment Tests		End Semester Examination
		1	2	
Remember	K1	10	10	10
Understand	K2	20	20	20
Apply	K3	20	20	70
Analyse				
Evaluate				
Create				

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks

Assignment/Quiz/Course project : 15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1): Explain various components of a communication system**.**

1. What is the need of a modulator in a radio communcation system?
2. What are the various frequency bands used in radio communication
3. Why base band communication is infeasible for terrestrial air transmission?

Course Outcome 2 (CO2): Discuss various sources of noise, and its the effect in a communication system**.**

1. What is thermal noise?
2. Describe the noise voltage generated across resistor?
3. Why is it that noise voltage can not be used as a source for power?

Course Outcome 3 (CO3): Explain amplitude modulation and its variants for a sinusoidal message**.**

1. Write down the equation for an AM wave for a sinusoidal message
2. What is the significance of modulation index?
3. Describe envelope detector

Course Outcome 4 (CO4): Explain frequency modulation and its variants for a sinusoidal message

4. How is practical bandwidth for an FM wave determined?
5. What are the value of frequency devaiation, bandwidth for a typical FM station?
6. What is PLL?

Course Outcome 5 (CO5): List and compare various transmitter and receiver systems of AM and FM

1. Draw the block diagram of a super heterodyne receiver.
2. How is adjasecent channel rejection achieved in superhet? How is image rejection achieved in a superhet?
3. Explain the working principle of one FM generator, and one FM demodulator.

Syllabus

Module I

Introduction, Elements of communication systems, Examples of analog communication systems, Frequency bands, Need for modulation.

Noise in communication system, Definitions of Thermal noise (white noise), Various types of noise -- Shot noise, Partition noise, Flicker noise, Burst noise, (No analysis required) Signal to noise ratio, Noise factor, Noise temperature, Narrow band noise.

Module II

Brief overview of signals and systems – Signals, Classification of signals, Energy and power of signals, Basic signal operations, Impulse function, Properties of impulse function, Convolution, LTI system, Fourier Transform, Basic properties, Using Fourier transform to study LTI system.

Module III

Amplitude modulation (AM), Double-side band suppressed carrier (DSB-SC) modulation Single sideband modulation (SSB) – spectrum, power, efficiency of all the three variants. (Study of only tone modulation in DSB-SC, AM, and SSB.) Amplitude-modulator implementations – switching modulator, balanced modulator. AM demodulators -- Coherent demodulator. Envelope detector.

Module IV

Frequency modulation – modulation index, frequency deviation, average power, spectrum of tone modulated FM. Heuristics for bandwidth of FM. Narrow band FM and wide-band FM. FM generation: Varactor diode modulator, Armstrongs method. FM demodulation – slope detection, PLL demodulator.

Module V

Superheterodyne reciever, Principle of Carrier synchronization using PLL, NTSC Television broadcasting.

Text Books

1. Kennedy, Davis, “Electronic Communication Systems,” 4th Edition, Tata McGraw Hill

2. Wayne Tomasi, “Electronic Communication Systems – Fundamentals through Advanced,” 5th edition, Pearson.

3. B. P. Lathi, Zhi Ding, Modern Digital and Analog Communication Systems, 4th edition, Oxford University Press.

Reference books

1. Leon W. Couch, Digital and Analog Communication Systems, 8th edition, Prentice Hall.

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
I	Introduction, Elements of communication systems, Examples of analog communication systems, Frequency bands, Need for modulation	3
	Noise in communication system, Definitions of Thermal noise (white noise), Shot noise, Partition noise, Flicker noise, Burst noise, (No analysis required) Signal to noise ratio, Noise factor, Noise temperature, Narrow band noise.	5
II	**Brief Overview of Signals and Systems:** Signals, Classification of signals, Energy and power of signals, Basic signal operations,	4
	Impulse function, Properties of impulse function, Convolution,	2
	Definition of Linear time-invariant system. Input-output relation of LTI system	2
	Definition of Fourier Transforms, Some Properties of Fourier Transform – Linearity, Time-shift, Modulation theorem, Parsevals theorem. Using Fourier Transform to study LTI systems.	5
III	Amplitude modulation (AM) – modulation index, spectrum, power, efficiency.	2
	Double-side band suppressed carrier (DSB-SC) modulation – spectrum, power, efficiency.	1
	Single sideband modulation (SSB) – spectrum, power, efficiency. (Study of only tone modulation in DSB-SC, AM, and SSB.)	1
	Amplitude-modulator implementations – switching modulator, balanced modulator (at block diagram level).	2
	AM demodulators -- Coherent demodulator. Envelope detector.	3
IV	Frequency modulation – modulation index, frequency deviation, average power, spectrum of tone modulated FM	4
	Heuristics for bandwidth of FM. Narrow band FM and wide-band FM.	1
	FM generation: Varactor diode modulator, Armstrongs method. FM demodulation – slope detection, PLL demodulator.	4

V	Receivers for AM/FM: Super heterodyne receiver (block diagram), Adjacent channel selectivity, Image rejection, Double conversion.	3
	Carrier Synchronization using PLL	1
	NTSC Television broadcasting using AM, FM radio broadcasting.	2

Sample Assignments

1. Using the message signal m(t)=t /1+t^2. Determine and sketch the modulated wave for amplitude modulation whose percentage of modulation equal the following values – 50%, 100%, 120%
2. A standard AM transmission sinusoidally modulated to a depth of 30% produces sideband frequencies of 4.98MHz & 4.914 MHz. the amplitude of each sideband frequency is 75V. Determine the amplitude and frequency of the carrier?
3. Write the typical frequency ranges for the following classification of EM spectrum: MF, HF,VHF and UHF.
4. List the basic functions of a radio transmitter and corresponding functions of the receiever?
5. Discuss the types causes and effects of various forms of noise at a receiver.
6. What are the different frequency components in SSB & DSBSC signals?
7. Describe the AM generation using diode as a nonlinear resistor.
8. Define the following terms in the context of FM -- Frequency deviation, frequency sensitivity, instantaneous phase deviation.
9. The equation for FM wave is s(t)= 10 Cos $(2\pi * 10^6 t + 5 \sin(200\pi t + 10 \sin(3000\pi t))$ Calculate frequency deviation, approximate transmission BW and power in the modulated signal.

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH. DEGREE EXAMINATION

ECT 283: Analog Communication

Max. Marks: 60 Duration: 3 hours

PART A

Answer all questions. Each question carries 3 marks each.

1. Explain the need for modulation.
2. A receiver connected to an antenna whose resistance is 50 ohm has an equivalent noise resistance of 30 ohm .calculate receiver noise figure in decibels & its equivalent noise temperature?
3. Plot the signal x(t)=u(t+1)+2u(t)-u(t-3)
4. State Parseval's theorem for DTFT. What is its signifance?
5. Define amplitude modulation? Give the frequency spectrum for AM wave?
6. Derive the expression for total power of AM wave?
7. Explain the following terms a)Modulation index b)Instantaneous frequency deviation
8. Compare AM & FM systems.
9. What are the advantages that the super heterodyne receiver has over the receivers? Are there any disadvantages?
10. Give the limitations of NTSC systems?

PART B

11. (a) Explain the following (i) Thermal noise (ii) Flicker noise (6 marks)
    (b) Explain the elements of communication systems in detail? (8 marks)

OR

12. (a) Define the signal to noise ratio and noise and noise figure of a receiver? How noise temperature related to noise figure? (8 marks)
    (b) List the basic functions of a radio transmitter & the corresponding functions of the receiver? (6 marks)
13. (a) Distinguish between energy & power signals. Give an example for each category? (6 marks)
    (b) State and prove the linearity and time shifting property of Fourier Transform? (8 marks)

OR

14. (a) Check whether the systems are linear & stable. (i) $y(t)=e^{x(t)}$ (ii) y[n]=x[n-1] (6 marks)

    (b) Find convolution of signal x[n] = [1,-1, 1, 1] with itself? (5 marks)
    (c)Distinguish between causal & non causal systems with suitable examples? (3 marks)

OR

15. (a) Derive the expression of total power in SSB wave? (7 marks)

(b) Describe the AM demodulation using envelope detector? (7 marks)

OR

16. (a) Describe the DSB SC wave generation process using balanced modulation (9 marks)

(b) Give the spectrum of SSB & DSB SC waves? Make comparison of bandwidth requirements. (5 marks)

17. (a) Explain the direct method of generating FM signal using varactor diode? (6 marks)
(b) Explain frequency modulation and it average power? (6 marks)

OR

18. (a) Explain with relevant mathematical expressions, the demodulation of FM signal using PLL? (10 marks)
(b) Give the spectrum of tone modulated FM? (4 marks)

19. (a) Explain the super heterodyne receiver with a detailed block diagram? (10 marks)
(b) Explain how the use of RF amplifier & improve the NR of a super heterodyne receiver? (4 marks)

OR

20. (a) Explain the TV broadcasting system using AM? (10 marks)
(b) What is image frequency, how does it arise? (4 marks)

Simulation Assignments

The following simulations can be done in Python/SCILAB/MTLAB or LabVIEW.

Amplitude Modulation Schemes

- Create a sinusoidal carrier($x_c(t)$) and AF signal(x_t) with the frequency of carrier being 10 times that of the AF signal.
- Compute the AM signal as $mx_c(t)x(t) + x_c(t)$ for various values of the modulation index m ranging from 0 to 1.
- Observe the power spectral density of this AM signal.
- $mx_c(t)x(t)$ is the DSB-SC signal. Observe this signal and its power spectral density.
- Load a speech signal in say in *.wav* format into a vector and use it in place of the AF signal and repeat the above steps for a suitable carrier.

SSB Signal Generation

- Simulate an SSB transmitter and receiver using $-\frac{\pi}{2}$ shifters. This can be realized by the Hilbert Transform function in Python, MATLAB etc.
- Test the system with single tone and speech signal.
- Add channel noise to the signal and test for the robustness against noise.
- Slightly offset the receiver carrier phase and observe the effect at the reception.

FM Signal Generation

- Create a sinusoidal carrier($x_c(t)$) and a single tone signal ($x(t)$) with the frequency of carrier being 50 times that of the message tone.
- Compute the FM signal with a modulation index of 5.
- Observe the power spectral density of this FM signal for spectral width of 10 times that tone frequency.

AM Radio Receiver

- Procure a radio kit
- Assemble the kit by soldering all components and enjoy.

FM Radio Receiver

- Procure an FM radio kit
- Assemble the kit by soldering all components and enjoy.

Generation of Discrete Signals

- Generate the following discrete signals
  - Impulse signal
  - Pulse signal and
  - Triangular signal

ECT285	INTRODUCTION TO SIGNALS AND SYSTEMS	CATEGORY	L	T	P	CREDIT
		Minor	3	1	0	4

Preamble: This course aims to apply the concepts of electrical signals and systems

Prerequisite: None

Course Outcomes: After the completion of the course the student will be able to

CO 1	Define and classify continuous and discrete signals
CO 2	Explain and characterize a system and LTI system
CO 3	Explain the spectrum of a signal

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	3			2							
CO 2	3	3		3	2							
CO 3	3	3		3	2							

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember	10	10	20
Understand	10	10	20
Apply	30	30	60
Analyse			
Evaluate			
Create			

Continuous Internal Evaluation Pattern:

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1): Definition and classification of signals

1. Define a signal. Classify them to energy and power signals.
2. Determine whether the signal x(t)=cos(3t)+sin(5t) is periodic. If so what is the period?
3. Compare the frequency range of continuous time and discrete signals.

Course Outcome 2 (CO2): Explain and characterize a system

1. Check whether the system y[n]=cos{x[n]}is a. Stable b. Causal c. time invariant d. linear
2. Derive the ouptut of a continuous time LTI system
3. Give the meaning of impulse response of LTI systems

Course Outcome 2 (CO3): Spectra of Signals

1. State and prove Parsevals theorem
2. State and prove the modulation property of Fourier transform
3. Find the continuous tiime Fourier transform a pulse of width w and amplitude unity and centred about the origin.

Syllabus

Module 1 : Introduction to Continuous Time Signals

Definition of signal. Basic continous-time signals. Frequency and angular frequency of continous-time signals . Basic operation on signals. Classification of continous-time signals:Periodic and Non-periodic signals.Even and Odd signals, Energy and power signals. Noise and Vibration signals.

Module 2 : Discrete Time Signals

Basic discrete-time signals. Frequency and angular frequency of discrete-time signals.Classification of discrete-time signals:Periodic and Non-periodic signals.Even and Odd signals, Energy and power signals.

Module 3: Systems

System definition. Continuous-time and discrete-time systems. Properties – Linearity, Time invariance, Causality, Invertibility,Stability. Representation of systems using impulse response.

Module 4: Linear time invariant systems

LTI system definition. Response of a continous-time LTI system and the Convolutional Integral. Properties. Response of a discrete-time LTI system and the Convolutional Sum. Properties. Correlation of discrete-time signals

Module 5 : Frequency analysis of signals

Concept of frequency in continous-time and discrete-time signals. Fourier transform of continuous-time and discrete-time signals. Parsevals theorem. Interpretation of Spectra. Case study of a vibration signal.The sampling theorem.

Text Books

1. Simon Haykin, Barry Van Veen, Signals and systems, John Wiley
2. Hwei P.Hsu, Theory and problems of signals and systems, Schaum Outline Series, MGH.
3. Anders Brandt, Noise and Vibration Analysis,Wiley publication.
4. A Anand Kumar, Signals and systems, PHI learning
5. Sanjay Sharma, Signals and systems

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**Introduction to Continuous Time Signals**	
1.1	Definition of signal, Basic continous-time signals.	3
1.2	Frequency and angular frequency of continous-time signals	1
1.3	Basic operation on signals	1
1.4	Classification of continous-time signals	3
1.5	Noise and Vibration signals	1
2	**Discrete Time Signals**	
2.1	Basic discrete-time signals and its frequency	3
2.2	Classification of discrete-time signals	3

3	**Systems**	
3.1	System definition- CTS & DTS	1
3.2	Properties-Linearity, Time invariance	3
3.3	Causality, Invertibility, Stability	2
3.4	Representation of systems using impulse response	1
4	**Linear time invariant systems**	
4.1	LTI system definition.Properties.	1
4.2	Response of a continuous-time LTI system and the Convolutional Integral	3
4.3	Response of a discrete-time LTI system and the Convolutional Sum	3
4.4	Correlation of discrete-time signals	2
5	**Frequency analysis of signals**	
5.1	Concept of frequency in continuous-time and discrete-time signals	1
5.2	CTFT and spectra	3
5.3	DTFT and spectra	3
5.4	DFT	1
5.5	Parsevals theorem	1
5.6	Case study of a vibration signal	1
5.7	The sampling theorem	2

Model Question Paper

A P J Abdul Kalam Technological University

Fourth Semester B Tech Degree Examination

ECT 285 Introduction to Signals and Systems

Time: 3 Hrs **Max. Marks: 100**

PART A

Answer All Questions

1	Differentiate between energy and power signal with example.	(3)	K_2
2	Find the even and odd components of $x(t) = e^{jt}$.	(3)	K_2
3	Define discrete time signal and comment about its frequency range.	(3)	K_2
4	Sketch the sequence $x(n) = 2\delta(n-3) - \delta(n-1) + \delta(n) + \delta(n+2)$.	(3)	K_2
5	State and explain BIBO condition for system.	(3)	K_1
6	Distinguish between continuous time and discrete time systems.	(3)	K_2
7	Derive a relationship between input and output for a discrete LTI system	(3)	K_2
8	Compute the energy of the signal $x(n) = 0.8^n u(n)$	(3)	K_2
9	State and explain sampling theorem.	(3)	K_2
10	Comment about the input output characteristics of continuous time Fourier transform	(3)	K_2

PART B

Answer one question from each module. Each question carries 14 mark.

11(A)	Determine whether or not the signal $x(t) = \cos t + \sin \sqrt{2}t$ is periodic. If periodic determine its fundemental period.	(7)	K_2
11(B)	Define, sketch and list the properties of continuous time impulse function	(7)	K_2

OR

12(A)	Determine whether the signal $x(t) = e^{-2t}u(t)$ is energy signal, power signal or neither.	(7)	K_2
12(B)	Define unit step function and plot $u(t+2) - u(t-2)$.	(7)	K_2
13(A)	Given the sequence $x(n) = \{1, 2, 1, 1, 3\}, -1 \leq n \leq 3$. Sketch • $x(-n+2)$ • $x(n/2)$	(8)	K_3
13(B)	Show that any signal $x(n)$ can be represented as the summation of an even and odd signal.	(6)	K_2

OR

14	Discuss briefly the basic discrete time signals.	(14)	K_2
15(A)	Explain linear and nonlinear systems.	(6)	K_2
15(B)	Apply the properties of system to check whether the following systems are linear or nonlinear • $y(t) = tx(t)$ • $y(n) = x^2(n)$	(8)	K_3

OR

16(A)	A sytem has an input-output relation given by $y(n) = T\{x(n)\} = nx(n)$. Determine whether the system is a)Memoryless b)Causal c) Linear d) Time invariant e)Stable	(14)	K_3

17	The impulse response of a linear time invariant system is $h(n) = \{1, 2, 1, -1\}, -1 \leq n \leq 2$ Determine the response of the system for the input signal $x(n) = \{1, 2, 3, 1\}$	(14)	K_3

OR

18	A system is formed by connecting two systems in cascade. The impulse response of the system is given by $h_1(t)$ and $h_2(t)$ respectively where $h_1(t) = e^{-2t}u(t)$ and $h_2(t) = 2e^{-t}u(t)$ a)Find overall impulse response h(t) of the system. b) Determine the stability of the overall system	(14)	K_3
19(A)	Find the Nyquist rate of $x(t) = sin400\pi t + cos500\pi t$.	(7)	K_2
19(B)	State and prove modulation property of Fourier Transform	(7)	K_2

OR

20(A)	Find the CTFT of the signal $x(t) = te^{-at}u(t)$	(7)	K_2
20(B)	State and prove Parsevals theorem	(7)	K_2

Simulation Assignments

The following simulation assignments can be done with Python/MATLAB/ SCILAB/OCTAVE

1. Generate the following discrete signals
   - Impulse signal
   - Pulse signal and
   - Triangular signal
2. Write a function to compute the DTFT of a discrete energy signal. Test this function on a few signals and plot their magnitude and phase spectra.
3. - Compute the linear convolution between the sequences $x = [1, 3, 5, 3]$ with $h = [2, 3, 5, 6]$. Observe the stem plot of both signals and the convolution.
   - Now let $h = [1, 2, 1]$ and $x = [2, 3, 5, 6, 7]$. Compute the convolution between h and x.
   - Flip the signal x by 180° so that it becomes $[7, 6, 5, 3, 2]$. Convolve it with h. Compare the result with the previous result.
   - Repeat the above two steps with $h = [1, 2, 3, 2, 1]$ and $h = [1, 2, 3, 4, 5, 4, 3, 2, 1]$
   - Give your inference.
4. - Write a function to generate a unit pulse signal as a summation of shifted unit impulse signals
   - Write a function to generate a triangular signal as a convolution between two pulse signals.
5. - Relaize a continuous time LTI system with system response

$$H(s) = \frac{5(s+1)}{(s+2)(s+3)}$$

   . One may use *scipy.signal.lti* package in Python.
   - Make it into a discrete system (possibly with *scipy.signal.cont2discrete*)
   - Observe the step response in both cases and compare.